Curriculum M. Tech. VLSI Design
2025-26 Batch Onwards

VISION of the Department:

The Department aims to be recognized as centre of excellence in Electronics and Communication Engineering by continuously striving to achieve excellence in providing Education, Research, and Innovation**.**

MISSION of the Department:

1. To provide our graduates with state of art facilities, experienced engineering education that balances both theoretical and practical knowledge for the design, analysis and operation of electronic systems in order to meet the needs of the relevant industry and research organization.
2. To conduct research in the field of Electronics and Communication Engineering focusing in the emerging research areas such as advanced communication systems, VLSI, Photonics systems, embedded systems etc.
3. To promote the overall development of graduates by encouraging them to participate in co-curricular and extra-curricular activities & providing awareness of ethical values in order to prepare them to face the challenges of the changing world.
4. To build relationship with Alumni to create a network and support for the department.
5. To design the curriculum through a continuous process in consultation with stakeholders so that the students graduating from the department have top rating in placement.

PEOs, POs, and PSOs M.Tech
(VLSI Design)

Programme Educational Objectives

This programme prepares graduates to

1. Be technically competent in design, development and implementation of electronics and VLSI design and extends into applications in the different thrust areas.
2. Possess suitable knowledge for analysing, modelling, and evaluating the research problems in major thrust areas of VLSI design.
3. Possess interpersonal skills, team work capabilities, communication skills, leadership and awareness of the social, ethical and legal responsibilities leading to lifelong learning and career development.
4. Be successfully employed in electronics profession in industry/ research organization and to have entrepreneurial skill.

Program Outcomes (POs):

1. An ability to independently carry out research /investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

Programme Specific Outcome (M.Tech (VLSI DESIGN))

1. Ability to attain, identify and apply knowledge of mathematics, science & engineering in Electronics VLSI design discipline to the solution of various engineering problems.
2. Ability to develop the design capability among students so that they have the ability to participate in creative, synthetic and integrative activities of the relevant branch of engineering.
3. Ability to use techniques and modern CAD Tools so as to implement them in engineering practice to develop professional skills that will prepare the students for immediate employment in the relevant branch of engineering in industry.

Semester wise PG Scheme for M.Tech. Programme (VLSI Design)
w.e.f. 2025-26 session

SEMESTER-I

Sr. No.	Course Stream	Course Name - Course Code	Credits	L-T-P
1.	Program Core Course	IC Fabrication **(EV1101)**	3	2-0-2
2.	Program Core Course	Digital VLSI Design **(EV1102)**	3	2-0-2
3.	Program Core Course	Semiconductor Devices **(EV1103)**	3	3-0-0
4.	Deptt. Elective Course (DEC-I)	• Low Power Sub-System Design & Technology **(EV1201)**	3	2-0-2
		• Semiconductor Memory Design & Applications **(EV1202)**		2-0-2
		• FPGA Based System Design **(EV1203)**		2-0-2
		• MEMS & NEMS **(EV1204)**		3-0-0
		• Flexible Electronics **(EV1205)**		3-0-0
5.	Design of experiments and research methodology	Design of experiments and research methodology **(EV1001)**	3	2-0-2
6.	Soft Computing /Soft Skills & Management	Soft Computing /Soft Skills and Management **(SM1001)**	3	
		Total Credits	**18**	

SEMESTER-II

Sr. No.	Course Stream	Course Name - Course Code	Credits	L-T-P
1.	Program Core Course	System Hardware Design **(EV1104)**	3	2-0-2
2.	Program Core Course	Semiconductor Device Modelling **(EV1105)**	3	2-0-2
3.	Program Core Course	Analog and Mixed Signal VLSI Design **(EV1106)**	3	2-0-2
4.	Deptt. Elective Course (DEC-II)	• Real Time Embedded System **(EV1251)**	3	2-0-2
		• Optoelectronic Materials and Devices **(EV1252)**		3-0-0
		• Semiconductor Packaging **(EV1253)**		3-0-0
		• Radio Frequency Integrated Circuits (RFIC) **(EV1254)**		3-0-0
		• CAD for VLSI **(EV1255)**		2-0-2
		• Testing & Fault Tolerance **(EV1256)**		3-0-0
5.	Open Elective	• Neural Networks **(EV3001)**	3	3-0-0
		• Flexible Electronics **(EV3002)**		3-0-0
		• Neuromorphic Engineering **(EV3003)**		3-0-0
		• Sensors & Actuators **(EV3004)**		3-0-0
6.	Engineering Mathematics		3	
7.	Industrial Tour	**EV4001**		
		Total Credits	**18**	

SEMESTER -III

Sr. No.	Course Name /Course Code	Credits
1.	Seminar and Report Writing **(EV5001)**	2
2.	Research and Publication Ethics **(RP6001)**	2
3.	Dissertation-I **(EV7001)**	14
	Total	**18**

SEMESTER-IV

Sr. No.	Course Name /Course Code	Credits
1.	Dissertation-II **(EV8001)**	18
	Total	**18**

SEMESTER-I
(CORE COURSES)

Course Name	**:**	**IC FABRICATION**
Course ID	**:**	**EV1101**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Course Objectives:

Students should be able

- To develop the basic understanding of device fabrication technique, device performance, and intended applications.
- To explore the fundamental concepts of MOS device integration as well as the benefits and drawbacks of emerging technology that will be employed in future devices.
- To characterize new materials, study methods and tools for VLSI devices, circuits, and systems.
- To gain hands-on introduction on the fabrication of integrated circuits.

Total No. of Lectures- 28

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** Modern Semiconductor IC fabrication Industrial/Academic Landscape, Introduction of Semiconductor Ecosystem (Foundry/Fab, IP design house, Chip design house, EDA Vendors), Foundries in the India and abroad, Overview of modern CMOS process flow – basic steps Crystal growth and wafer basics Cleanroom basics – environment, infrastructure, PDK (Process design kit), PVT (Process, voltage and temperature) corner in VLSI & its effects on multiple dies on a single wafer (effects on performance, defects, yield).	4
Unit 2	**PHYSICAL VAPOR DEPOSITION** Thermal evaporation, Resistive Evaporation, Electron beam evaporation, Laser ablation, Sputtering. Chemical Vapor Deposition: Different kinds of CVD techniques: APCVD, LPCVD, PECVD, ALD. Epitaxial layer growth, molecular beam epitaxy, merits and demerits among epitaxial processes; recent trends in Epitaxy.	6
Unit 3	**OXIDATION, DIFFUSION AND ION IMPLANTATION** Oxidation process, Diffusion process, Limitations of Diffusion, Ion Implantation, Applications in ICs, Ion Implantation System, Ion Implantation Damage, Annealing process.	6
Unit 4	**OTHER TECHNIQUES FOR THIN FILM DEPOSITION** Sol-gel method, Microemulsion, Vapor liquid solid growth, spray pyrolysis, template-based synthesis, doctor blade technique, mechanical exfoliation techniques for 2D materials.	5
Unit 5	**LITHOGRAPHY TECHNIQUES** Optical lithography, electron beam lithography, x-ray lithography, ion beam lithography, maskless lithography; resists and mask preparation, etching; types of etching- wet and dry etching; Piranha Etching, dry etching techniques, reactive ion etching (RIE), Deep reactive ion etching (DRIE), Etch stop techniques, recent trends in etching, Surface and bulk micromachining, LIGA process.	3
Unit 6	**SEMICONDUCTOR DEVICE CHARACTERIZATION** Fundamentals of Electrical Characterizations, two probe and four probe methods, SMU's, CVU's, two and four terminal device characterization, Fundamentals of Material Characterizations: XRD, AFM, SEM, TEM.	4

List of Experiments		No. of turns
1	Working in cleanroom environment, protocols, wafer handling.	2
2	Pattern transfer using lithography techniques.	2
3	To perform wet and dry etching techniques.	2
4	Thin film deposition using thermal evaporation or E-beam evaporation technique.	2
5	To perform material characterizations through SEM	2
6	Fabrication and characterization of MOS device	4

Course Outcomes: By the end of this course, the students will be able to	
1	Work in the cleanroom environment for semiconductor device fabrication.
2	Recognize the basic operation principles of semiconductor fabrication equipment.
3	Analyze IC fabrication methodologies and evaluate component effects on IC design for VLSI and ULSI domains.
4	Demonstrate in-depth knowledge in wafer preparation, lithography and etching, diffusion process, material, device characterization and electrical measurement technique.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)	2021
2	Introduction to Nanotechnology Risal Singh & Shipra Mittal Gupta (Oxford India Press)	2016
3	Plummer, Deal, Griffin "Silicon VLSI Technology: Fundamentals, Practice & Modelling" PHI.	2001
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Fundamentals of Microfabrication and Nanotechnology by Marc Madou, (CRC Press)	Latest Edition
2	VLSI Fabrication Principles: Silicon and Gallium Arsenide, S. K. Gandhi, John Wiley and Sons	Latest Editon

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	Semiconductor Devices for Next Generation Field Effect Transistors (More than Moore): A Physics Perspective by Prof. Nandita Das Gupta, IIT Madras https://archive.nptel.ac.in/courses/117/106/117106093/	**NPTEL**
2	Fabrication of Silicon VLSI Circuits using the MOS Technology by Prof. A.N Chandorkar, IIT Bombay https://archive.nptel.ac.in/courses/108/101/108101089/	**NPTEL**

CO-PO Mapping:

CO	PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	H	M	H	H	M	H
CO2	H	M	H	H	H	M
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	H

Course Name	**:**	**DIGITAL VLSI DESIGN**
Course ID	**:**	**EV1102**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Course Objectives:

Students should be able

- To explain the static and dynamic power dissipation in CMOS circuits.
- To design combinational and sequential CMOS circuits.
- To describe the effect of interconnects on crosstalk and delay.
- To comprehend static and dynamic CMOS logic circuits.
- To illustrate the design, the schematic and layout of Digital VLSI Circuits and carry out various analysis using CAD tools.

Total No. of Lectures – 28

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** ASIC design flow, Basics of Layout, DRC rule, metal stack, and different metal layers in the layout, Aging in VLSI circuits.	3
Unit 2	**CMOS INVERTER AND PERFORMANCE ESTIMATION** Inverter layout, Static characteristics, dynamic behavior, power consumption, comparison of CMOS inverter performance with different beta ratios, buffer design using the method of logical effort, logical effort, parasitic delay, Interconnect parameters, resistance and capacitance, distributed RC delay, Delay Estimation, RC delay models, Linear delay Models.	7
Unit 3	**COMBINATIONAL LOGIC** Static CMOS Design, Synthesis of complex CMOS Gates, Ratioed Logic, Pass Transistor Logic, various logic circuits using pass transistors. Dynamic CMOS Design: Dynamic Logic, basic principles, DOMINO Logic, NORA- CMOS logic.	7
Unit 4	**SEQUENTIAL LOGIC** Static latches and flip-flops (FFs), dynamic latches and FFs, Clock strategies for sequential design, sense-amplifier based FFs, Schmitt trigger, monostable and astable circuits.	5
Unit 5	**APPLICATION OF LOGIC GATES** Overview of Logic gates/Standard cells used in industry (inverter, Latch, FF, clock cells, well tap cells, End cap cells, filler cells, fillcap, cells, level shifter etc.), Different type of Logic libraries (RVT, LVT, HVT, PMK etc.) and their utilization in SOC or CPU design (through synthesized Verilog netlist), Cell Placement & Routing, Static timing analysis (setup, hold, slack, clock skew etc), case study from cadence e-learning resources.	6

List of Experiments		**No. of turns**
1	Familiarization with Simulation Software for schematic, layout entry and circuit simulation, SPICE Modeling, GDSII.	2
2	Capture the schematic of CMOS inverter and compute the following from simulation results: a. t_{pHL}, t_{pLH} and t_d. b. Tabulate the delay and find the best geometry for minimum delay for CMOS inverter.	2
3	Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations.	2
4	Capture the schematic and layout of 2-input CMOS NAND, NOR and XOR gate having best	2

	geometry of CMOS inverter computed in experiment 1.	
5	Design and analyze the characteristics of a 3 input NAND gate using Dynamic Logic gate and DOMINO Logic style.	2

6	Design and analyze the characteristics of a positive and negative edge SR Latch, D flip flop and 4-bit register.	4

Course Outcomes: By the end of this course, the students will be able to	
1	Design and analyze various static and dynamic combinational logic circuit techniques.
2	Compute and estimate the power consumption and delay of a Digital VLSI circuits.
3	Explain various MOS sequential circuits.
4	Study and analyze interconnect parameters and various Interconnect Models on crosstalk delay and noise.
5	Design and analyze the layout and schematics of various digital VLSI circuits using CAD tools.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Digital Integrated Circuits – A Design Perspective, J.M. Rabaey, A.P. Chandrakasen and B. Nikolic, Pearson Education 2nd ed.	Latest edition
2	CMOS Digital Integrated Circuits – Analysis and Design, S. Kang and Y. Leblebici, Tata McGraw Hill 3rd ed.	2008
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	CMOS VLSI Design: A Circuits and Systems Perspective, N.H.E. Weste and K. Eshraghian, Addision Wesley 2nd ed.	1998
2	CMOS Circuit Design, Layout and Simulation, R.J. Baker, H. W. Lee, and D. E. Boyce, Wiley - IEEE Press 2nd edition.	2004

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	CMOS Digital VLSI Design by Prof. Sudeb Dasgupta, IIT Roorkee https://archive.nptel.ac.in/courses/108/107/108107129/	**NPTEL**

CO-PO Mapping Matrix:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	H	M
CO2	H	M	H	H	H	M
CO3	H	M	H	H	H	-
CO4	H	M	H	H	H	M
CO5	H	M	H	H	H	H

Course Name	**:**	**SEMICONDUCTOR DEVICES**
Course ID	**:**	**EV1103**
Credits	**:**	**3**
LTP	**:**	**3 0 0**

Course Objectives:

Students should be able

- To understand the physics of MOSFETS and interpret the device characteristics.
- To analyze MOSFET scaling challenges and non-classical device requirements.
- To examine the reliability issues for MOSFETs.
- To explore advanced MOSFET architectures and the concepts of emerging nanoscale devices

Total No. of Lectures: 42

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** Overview of CMOS Devices, Definition of Technology node, MOS Scaling theory, Issues in scaling MOS transistors: Short channel effects and quantum effects, Electrical contacts for MOSFETs, Requirements for Non classical MOS transistor.	6
Unit 2	**PHYSICS OF MOSFET** MOS capacitor, Energy Band Diagrams, CV characteristics, MOSFET: IV and CV characteristics, threshold voltage extraction methods, body effect, Channel Length Modulation, scaling of conventional MOSFETs and Short Channel Effects.	8
Unit 3	**RELIABILITY ISSUES** Role of interface quality and related process techniques, Gate oxide thickness scaling trend, SiO_2 vs High-k gate dielectrics. Integration issues of high-k, Interface states, bulk charge, band offset, stability, CV and IV techniques for interface reliability, Metal gate transistor: Motivation, requirements, Integration Issues.	8
Unit 4	**ADVANCE MOSFETS** Transport in Nano MOSFET, velocity saturation, quasi-ballistic and ballistic transport, injection velocity, velocity overshoot, SOI - PDSOI and FDSOI, Ultrathin body SOI – double gate transistors, integration issues. Vertical transistors - FinFET and gate all around FET, Metal source/drain junctions - Properties of Schottky junctions on Silicon, Germanium and compound semiconductors, Fermi level pinning.	10
Unit 5	**EMERGING DEVICES** Germanium Nano MOSFETs: strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors - material properties, MESFETs, Compound semiconductors, High electron mobility transistors (HEMTs), FETs based on novel materials, Single electron transistors, Self-switching diode, ballistic rectifiers, Schottky source-based FETs.	10

Course Outcomes: By the end of this course, the students will be able	
1.	To explain CMOS devices and technology scaling.
2.	To realize MOS capacitors, analyze MOSFET characteristics and apply scaling theory to MOSFETs.

3.	To analyze reliability issues in advanced MOS technology.
4.	To explain transport in nano MOSFETs and explore advanced transistor technologies.
5.	To design emerging devices and novel materials.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/Authors/Publisher**	**Year of Publication/ Reprint**
1	Fundamentals of Modern VLSI Devices, Y. Taur and T. Ning, Cambridge University Press.	2009
2.	S.M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley.	2007
3	K. Hess, Advanced Theory of Semiconductor Devices, Prentice-Hall.	1988
4	Yuan Taur & Tak H. Ning, Fundamentals of Modern VLSI Devices, Cambridge.	1998
5	Yannis Tsividis, Operation and Modelling of the MOS Transistor, Oxford University Press	2010
Reference Books:		
Sr. No.	**Name of Book/Authors/Publisher**	**Year of Publication/ Reprint**
1	Mark Lundstrom & Jing Guo, Nanoscale Transistors: Device Physics, Modelling & Simulation, Springer .	2005
2	J.P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Springer.	1997
3	Michael Shur, Physics of Semiconductor Devices, Prentice Hall.	1990
4	Research and review papers in specific area.	

Equivalent MOOC courses:

Sr. No.	**Course Links**	**Offered by**
1	Semiconductor Devices for Next Generation Field Effect Transistors (More than Moore): A Physics Perspective By Prof. Sudeb Dasgupta, IIT Roorkee https://onlinecourses.nptel.ac.in/noc25_ee75/preview	**NPTEL**
2	Nanoelectronics devices and materials by Prof. Navakanta Bhat, IISc Bangalore https://nptel.ac.in/courses/117108047	**NPTEL**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	H	H
CO2	H	M	H	H	H	H
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	H
CO5	H	M	H	H	H	H

SEMESTER-I
(DEPARTMENT ELECTIVE COURSES (DEC-I))

Course Name	**:**	**LOW POWER SUBSYSTEM DESIGN AND TECHNIQUES**
Course ID	**:**	**EV1201**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Course Objectives:

Students should be able

- To describe the sources of power dissipation and understand the impact of power on system, performance and reliability
- To explain the different approaches of low power design at Circuit level
- To understand the concept of static RAM architectures for low power.
- To explain adiabatic switching circuits and battery aware systems.

Total No. of Lectures – 28

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** Introduction, need for low power designs, sources of power dissipation: Dynamic Power Dissipation, Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation Degrees of Freedom. Emerging low power approaches, Impact of technology, and gate oxide thickness on power dissipation.	5
Unit 2	**SUPPLY VOLTAGE SCALING FOR LOW POWER** Introduction**,** Device feature size scaling, multi-level voltage scaling and challenges, Architectural level approaches: Parallelism, Pipelining; Voltage scaling using high-level transformations, Dynamic voltage scaling and frequency scaling, Power Management.	5
Unit 3	**SWITCHED CAPACITANCE MINIMIZATION APPROACHES** Introduction, system level approach: Hardware Software co-design, Bus Encoding, Two's complement Vs Sign Magnitude, Architectural optimization, clock gating, low power arithmetic circuits and advanced flip-flop and latch designs for power efficiency, gated-clock FSMs and logic styles for low power, Low power static RAM architectures.	12
Unit 4	**LEAKAGE POWER MINIMIZATION APPROACHES** Introduction, Variable-threshold-voltage CMOS (VTCMOS) approach, multi-threshold-voltage CMOS(MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS).	3
Unit 5	**SPECIAL TECHNIQUES FOR LOW POWER** Adiabatic Switching Circuits, Introduction to battery aware systems	3

List of Experiments:		**No. of turns**
1.	Design Adder and substractor circuit and ascertain power efficiency for the same	4
2.	Design a latch specifying some time constraints using universal gates and ascertain power efficiency for the same	2

3.	Design a low power CMOS SRAM cell at 90nm and 180nm technology node and compare its performance in terms of power	8

Course Outcomes: By the end of this course, the students will be able	
1.	To understand various sources of power dissipation in VLSI circuits.
2.	To analyze power in VLSI circuits based on supply voltage scaling and switched capacitance minimization approach
3.	To explain the various approaches to minimize leakage power.
4.	To design a low power circuit and analyze the power.
5.	To understand the special techniques for low power circuit design.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1.	A. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press.	1995
2.	Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers.	1995
3.	Ajit Pal, low power VLSI circuits and systems	Latest Edition
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Rabaey,J,M. and Pedram, M., Low power design methodologies, Springer.	1996
2	Roy, K. and Prasad, Sharat C., Low Power CMOS VLSI: Circuit Design, John Wiley.	2000
3	Research and review papers in specific area.	

Equivalent MOOCs courses:

Sr. No.	**Course Links**	**Offered by**
1	Low power VLSI circuits and systems By Prof. Ajit Pal (IIT Kharagpur) https://archive.nptel.ac.in/courses/106/105/106105034/	**NPTEL**
2	Design and Analysis of VLSI Subsystems, IIIT Bangalore By Prof. Madhav Rao https://onlinecourses.nptel.ac.in/noc25_ee18/preview	**NPTEL**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	H	H	H	H	H
CO2	H	H	H	H	H	H

CO3	H	H	H	H	H	H
CO4	H	H	H	H	H	H
CO5	H	H	H	H	H	H

Course Name	**:**	**SEMICONDUCTOR MEMORY DESIGN AND APPLICATIONS**
Course ID	**:**	**EV1202**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Course Objectives:

Students should be able

- To understand the basic concepts of memory, its types, memory hierarchy and associated design challenges
- To analyze the conventional volatile and non-volatile memories, their reliability issues and array structures
- To explore and evaluate the characteristics of emerging non-volatile memories
- To identify and discuss the role of memory in the state-of-art applications.

Total No. of Lectures- 28

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** Review of a computer system; Memory hierarchy; Semiconductor memory overview; Memory types, tradeoffs, and challenges; volatile & non-volatile memories.	5
Unit 2	**CONVENTIONAL VOLATILE MEMORIES AND NON-VOLATILE MEMORIES** Volatile memories - SRAM: Review of Device basic structure; memory unit cell operation; Array Operation; Reliability issues and Current Advances; DRAM: Review of Device basic structure; memory unit cell operation; Array Operation; Reliability. Non-volatile memory – FLASH memory, Floating Gate (FG) & Charge Trap (CT) flash; Flash memory physics; NAND vs NOR flash; Reliability and scaling issues; Current Advances: Nanocrystal; 3D NAND.	9
Unit 3	**EMERGING NON-VOLATILE MEMORIES** Resistive RAM (RRAM): Reliability; Unipolar and Bipolar; Filamentary & non-filamentary; Phase change memory (PCM); Conductive bridge RAM (CBRAM); Ferroelectric RAM (FeRAM); Spin-transfer Torque Magnetic RAM (STT-MRAM) eNVM performance comparison; eNVM challenges and opportunities to replace existing memory.	9
Unit 4	**MEMORY ARCHITECTURE AND APPLICATIONS** Conventional Memory architecture; Cross-point array architecture; Peripheral/control circuit; Sense amplifier; Memories for Neuromorphic computing, In-memory computing applications; Content addressable memory (CAM) applications, System-level implementation and challenges.	5

List of Experiments	**No. of turns**

1	Design SRAM cell and calculate it's noise margin for read, hold and write operation. Compare the SRAM cell at different technology nodes.	3
2	Design SRAM cell and calculate it's delay parameters. Compare the SRAM cell at different technology nodes in terms of rise time, fall time, and delay.	3

3	Design the layout of SRAM cell using Cadence Virtuoso and perform DRC, LVS.	2
4	Design DRAM cell and calculate it's delay parameter. Compare the DRAM cell different technology nodes.	3
5	To identify the problem statement, analyze and compare the various SRAM cell.	3

Course Outcomes: By the end of this course, the students will be able to	
1	Understand the basic concept of memory and design challenges.
2	Analyze and illustrate the schematic of a static and dynamic memory cell and explain in details the process of reading and writing a bit of information in it using CAD tools.
3	Explain the emerging non-volatile memories.
4	Investigate various memory architectures and applications of the memory cells.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Ashok K. Sharma," Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi	2007
2	Tegze P. Haraszti, "CMOS Memory Circuits", Kluwer Academic Publishers	2003
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Betty Prince, "Emerging Memories: Technologies and Trends", Kluwer Academic publishers	2002
2	Research and review papers in specific area.	

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	Not Available	

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	M	M
CO2	H	M	H	H	H	H
CO3	H	M	H	H	L	M
CO4	H	M	H	H	L	M

Course Name	**:**	**FPGA BASED SYSTEM DESIGN**
Course ID	**:**	**EV1203**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Course Objectives:

Students should be able

- To understand architecture and different technologies to configure FPGA.
- To develop test benches to simulate combinational and sequential circuits.
- To explore the development and deployment of FPGA based digital systems.
- To explore the working of advanced FPGA architecture.

Total No. of Lectures- 28

Lecture wise breakup		**No. of Lectures**
Unit 1	**FUNDAMENTAL CONCEPTS OF FPGA** Introduction to FPGA, issues in FPGA system design: area, timing, power, FPGA vs ASIC, FPGA design flow, basic blocks of FPGA, Applications of FPGA.	4
Unit 2	**FPGA ARCHITECTURES** Fuse, Antifuse, PROM, EPROM, EEPROM, Flash and SRAM based FPGAs, Xilinx CPLD Architecture, Circuit Design of FPGA fabrics. Fine, medium and coarse-grained architectures. MUX and LUT-based logic blocks, Fast carry chain.	5
Unit 3	**PROGRAMMING (CONFIGURING) AN FPGA** Configuration files, configuration cells, programming using configuration port, JTAG in brief, programming using JTAG port.	6
Unit 4	**EMBEDDED BLOCKS IN FPGA AND LOGIC SYNTHESIS** Embedded RAMs, Embedded multipliers, adders, MACs, Embedded processor cores (hard and soft), Clock trees and clock managers, General- purpose I/O, Gigabit transceivers, Hard IP, Soft IP and Firm IP, System gates versus real gates, Commercial EDA tools for synthesis.	6
Unit 5	**ADVANCED FPGA ARCHITECTURES** Xilinx Virtex (Architecture) FPGA, Kintex-7/Zynq-7000, Spartan, Pynq.	7

List of Experiments		**No. of turns**
1	Introduction to Verilog, synthesis, FPGA kits.	1
2	Develop a Verilog test bench code for testing and implement addition, subtraction, multiplication and division on FPGA kit.	2
3	Simulation, implementation and synthesis of digital circuits using Verilog in Xilinx ISE simulator of sequential logic	2
4	Design a sequence detector in Verilog and implement it on FPGA kit.	3
5	To implement real-time image recognition algorithms on FPGA for efficient visual data processing.	3
6	To implement real-time grayscale conversion of RGB images using FPGA for efficient image preprocessing.	3

Course Outcomes: By the end of this course, the students will be able to	
1	Understand the design model, methodologies, criteria and procedural steps involved in FPGA design.
2	Design, develop and simulate combinational and sequential circuits using test benches.
3	Implement digital circuits using FPGAs.
4	Explain the architecture of advanced FPGAs.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Wayne Wolf, FPGA - Based System Design, Pearson education, LPE 1st Indian Reprint	2004
2	Maxfield, Clive. The design warrior's guide to FPGAs: devices, tools and flows. Elsevier	2004
3	Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall PTR 2nd Ed	2010
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Steve Kilts, ―Advanced FPGA design – Architecture, Implementation and Optimization‖, Wiley publications	2007
2	Ron Sass and Andrew G. Schmidt, Morgan Kaufmann (MK), ―Embedded System design with Platform FPGAs‖, Elsevier,2010	2003

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	Digital System design with PLDs and FPGAs, IISc Bangalore by Prof. Kuruvilla Varghese **https://nptel.ac.in/courses/117108040**	**NPTEL**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	M	H
CO2	H	M	H	H	H	H
CO3	H	M	H	H	H	H
CO4	H	M	H	H	M	M

Course Name	**:**	**MEMS AND NEMS**
Course ID	**:**	**EV1204**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To understand MEMS and NEMS technologies, materials, and fabrication techniques.
- To analyse and design various MEMS devices such as switches, inductors, capacitors, filters, and phase shifters.
- To gain knowledge on RF MEMS systems for microwave applications.
- To explore the design, modelling, and application of sensors in MEMS and NEMS platforms.

Total No. of Lectures – 42

Lecture wise breakup		**No. of Lectures**
Unit 1	**MEMS SWITCHES** Introduction to MEMS switches; Capacitive shunt and series switches: Physical description, Circuit model and electromagnetic modeling; Techniques of MEMS switch fabrication and packaging; Design of MEMS switches.	8
Unit 2	**RF MEMS** RF MEMS for microwave applications, MEMS technology and fabrication, Mechanical modeling of MEMS devices, MEMS materials and fabrication techniques.	8
Unit 3	**MEMS INDUCTORS AND CAPACITORS** Micro machined inductors: Effect of inductor layout, Reduction of stray capacitance of planar inductors, Folded inductors, Variable inductors and polymer-based inductors; MEMS Capacitors: Gap-tuning and area-tuning capacitors, Dielectric tunable capacitors.	9
Unit 4	**MEMS FILTERS AND PHASE SHIFTERS** Modeling of mechanical filters, micro machined filters, Surface acoustic wave filters, Micro machined filters for millimeter wave frequencies; Various types of MEMS phase shifters; Ferroelectric phase shifters.	9
Unit 5	**MEMS- NEMS SENSORS** Thermal Sensor, Interaction of Thermal-Electrical Fields, Bio-MEMS Design Problems, Nano-Electro-Mechanical Systems (NEMS), NEMS Oscillators and Sensors, Optical MEMS/NEMS :2-D, 3-D Switches.	8

Course Outcomes: By the end of this course, the students will be able to	
1	Analyze the design principles, fabrication techniques, and materials used in RF MEMS for microwave applications.
2	Model and design MEMS switches with understanding of circuit and electromagnetic characteristics.
3	Evaluate and design MEMS inductors and capacitors for tunable applications with reduced parasitic.
4	Design and analyze MEMS filters and phase shifters for millimeter-wave frequency applications.
5	Explain the architecture, principles, and applications of MEMS and NEMS sensors including bio- and optical-domains.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Varadan, V.K., Vinoy, K.J. and Jose, K.J., "RF MEMS and their Applications", John Wiley & Sons.	2002
2	Rebeiz, G.M., "MEMS: Theory Design and Technology", John Wiley & Sons.	2003
3	De Los Santos, H.J, "RF MEMS Circuit Design for Wireless Communications", Artech House.	2006
4	Tai Ran Hsu, "MEMS and Microsystems Design and Manufacture", Tata McGraw Hill.	2002
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Madou, M., "Fundamentals of Microfabrication", CRC Press.	2001
2	Rebeiz, G.M., "RF MEMS: Theory Design and Technology", Wiley.	2003
3	Sze, S.M., "Semiconductor Sensors", John Wiley & Sons.	2002
4	Relevant Research Papers.	

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	A brief introduction of Micro – Sensors by Prof. Santanu Talukder, IISER Bhopal. https://onlinecourses.nptel.ac.in/noc25_ee01/preview	**Swayam**

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	M	H
CO2	H	M	H	H	H	H
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	H
CO5	H	M	H	H	M	H

Course Name	**:**	**FLEXIBLE ELECTRONICS**
Course Code		**EV1205**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To gain fundamental knowledge of thin-film materials and device physics for flexible and printed electronics.
- To describe key printing and deposition techniques for fabricating flexible devices.
- To perform circuit-level implementation and system integration on flexible substrates.
- To explore real-world applications, challenges, and future directions in flexible electronics and packaging.

Total No. of Lectures- 42

Lecture Wise Breakup		**No. of Lecture**
Unit 1	**INTRODUCTION TO FLEXIBLE AND PRINTED ELECTRONICS** Evolution of flexible electronics, review of cutting-edge research on flexible, plastic, stretchable, conformable or printed electronics. materials, components, and systems, applications for IoT.	8
Unit 2	**MATERIALS, PROCESSING, AND MANUFACTURING** Various semiconductors, dielectric, and conducting materials, Organic semiconductors; From chemical bonds to bands, Charge injection and transport, Examples of printable functional materials, Thin-film Deposition and Processing Methods for Flexible Devices, Solution-based Patterning Processes; Ink-jet printing, gravure and other processes, surface energy effects, multilayer patterning.	12
Unit 3	**FLEXIBLE THIN-FILM TRANSISTORS AND CIRCUITS** Thin-Film Transistor; Device structure and performance, Electrical characteristics, parameter extraction, characterization methods for rigid and flexible devices, electrical stability, printed transistors; Organic/polymer, metal-oxide, electrolyte gated, submicrometric OTFTs and gravure printed OTFTs, From transistors to circuits, circuits on flexible and non- silicon substrates, Contacts and Interfaces to Organic and Inorganic Electronic Devices, Schottky contacts, defects, carrier recombination, effect of applied mechanical strain.	12
Unit 4	**OTHER FLEXIBLE DEVICES AND SYSTEM INTEGRATION** Organic Light Emitting Diodes, flexible OLED displays and lighting, smart wallpaper, Organic Solar Cells, sensors, flexible batteries, supercapacitors, logic, memory, RFID tags, Latest applications, Encapsulation, roll to roll processes, Integration Issues, Designs for Future and case studies.	10

Course Outcome: By the end of this course, the students will be able to	
1	Explain the principles, materials, and physics behind thin-film and organic electronic devices used in flexible electronics.
2	Demonstrate knowledge of solution-based patterning, printing, and coating techniques and their applications in device fabrication.
3	Analyze and design thin-film transistors and circuits on flexible substrates, including the challenges in electrical characterization and mechanical strain.
4	Evaluate system-level integration, encapsulation, and performance issues in emerging flexible electronic applications like displays, sensors, and energy devices.

Suggested Books:

Text books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	"Large Area and Flexible Electronics", M. Caironi and Y.Y. Noh, WILEY-VCH.	2015
2	"Flexible Electronics: Materials and Applications", W. S. Wong, A. Salleo, Springer.	2009
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Organic and Printed Electronics: Fundamentals and Applications, G. Nisato, D. Lupo, S.Ganz, CRC Press.	2016
2	Organic Flexible Electronics: Fundamentals, Devices, and Applications, P. Coseddu and M. Caironi, Elsevier.	2020
3	Christoph Brabec, Ullrich Scherf, Vladimir Dyakonov (Editors), Organic Photovoltaics: Materials, Device Physics, and Manufacturing Technologies, Wiley VCH.	2014

Equivalent MOOC courses:

Sr. No.	**Course Links**	**Offered by**
1	Not available	

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	H	M	H	H	M
CO2	H	H	M	H	H	M
CO3	H	H	M	H	M	M
CO4	H	H	M	H	M	M

SEMESTER-II
(CORE COURSES)

Course Name	**:**	**SYSTEM HARDWARE DESIGN**
Course ID	**:**	**EV1104**
Credits	**:**	**3**
LTP	**:**	**2 0 2**

Course Objectives:

Students should be able

- To develop a comprehensive understanding of digital and embedded system design
- To understand the digital system design process and gain proficiency in Verilog, including hardware simulation and synthesis
- To understand FPGA architecture and implementation
- To analyze DSP processor architecture, ARM architecture and programming

Total No. of Lectures–28

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION TO DIGITAL AND EMBEDDED SYSTEMS DESIGN** Digital Design Using ROMs, PLAs and PLAs, BCD Adder, 32 - bit adder, A shift and add multiplier, Array multiplier, and Binary divider. Introduction to Embedded system, Design cycle in the development phase for an embedded system.	5
Unit 2	**Hardware Description Languages (HDL)** Digital system design process, Introduction to HDL(Verilog), Hardware Simulation, Hardware Synthesis, Levels of Abstraction, Characterizing Hardware Languages, Signal Assignments, Concurrent and Sequential Assignments.	5
Unit 3	**DESIGN ORGANIZATION AND PARAMETERIZATION** Definition and usage of Subprograms, Packaging Parts and Utilities, Design Parameterization, Design Configuration, Design Libraries. Type Declarations and Usage, Operators, Subprogram Parameter Types and Overloading, Predefined Attributes, User Defined Attributes. Dataflow Description: Multiplexing and Data Selection, State Machine Description. Behavioral Description of Hardware: Process Statement, Assertion Statement, Sequential Wait Statements.	5
Unit 4	**FPGA ARCHITECTURE** Designing and Implementation of Finite State Machines for FPGA; Synthesis Techniques and Timing Analysis; Placement and Routing; Embedded Hardware and Software Design with FPGA.	3
Unit 5	**DSP PROCESSOR ARCHITECTURE** Architecture; Functional Units; Fetch and Execute Packets; Pipelining; Registers Linear and circular Addressing Modes; Instruction Set Assembler Directives for TMS320C6x or ADSP21xx; Linear Assembly; ASM statement within C; Timers; interrupts; Multichannel Buffered Serial Ports; Direct Memory Access; Memory Considerations.	5
Unit 6	**ARM ARCHITECTURE AND ORGANIZATION** Architecture, Assembly Programming; THUMB Assembly Programming; ARM-THUMB Interworking; Assembly and C Mixed Programming; Exception Handling; ARM Tool chain (Assemblers, Compilers, Linkers & Debuggers).	5

List of Experiment		No. of turns
1.	Design and analysis of combinational logic circuits with Verilog using Xilinx ISE a. BCD Adder b. 4 bit binary to gray converter. c. Shift and add multiplier for 4-bit data. d. binary divider e. Multiplexer, de-multiplexer, comparator.	5
2.	Write Verilog code to describe the functions of a Full Adder using three modeling styles.	2
3.	Develop the Verilog code for the following flip-flops, SR, D, JK and T.	1
4.	Design a 4-bit binary, BCD counters (Synchronous reset and Asynchronous reset) and "any sequence" counters, using Verilog code.	2
5.	Design a sequence detector using Verilog code and verify using testbench.	2
6.	Write a Verilog code to model 32-bit ALU to perform 4 arithmetic and 4 logical operations and verify using testbench.	2

Course Outcomes: By the end of this course, the students will be able	
1.	To apply digital design techniques using ROMs, PLAs, BCD adders, 32-bit adders, etc. and also understand embedded system.
2.	To understand digital system design process using Verilog HDL
3.	To learn the usage of subprograms, packaging parts and utilities in design and also gain an understanding of design parameterization
4.	To design and implement Finite State Machines (FSM) on FPGA platforms
5.	To understand the architecture, functional units of DSP and ARM processors and their programming.

Suggested Books:

Textbooks:		
S. No.	**Name of Book /Authors / Publisher**	**Year of Publication/ Reprint**
1	Embedded System Design: Embedded System Foundations of Cyber-Physical Systems by Peter Marwedel, Springer	2010
2.	Embedded System Design: A Unified Hardware/Software introduction by Frank Vahid, Tony Givargis, John Wiley & Sons, Inc.	2001
3.	Verilog HDL: A Guide to Digital Design and Synthesis, S. Palnitkar, Prentice Hall NJ, USA	2003
4.	DSP Applications Using C and the TMS320C6x DSK, Rulph Chassaing, John Wiley & Sons, Inc.	2002
5.	ARM System-on-Chip Architecture, Furber, S., 2nd ed. Pearson Education.	2000

Reference Books:		
Sr. No.	**Name of Book/Authors/Publisher**	**Year of Publication/ Reprint**
1.	Digital Design and Computer Architecture, David Money Harris and Sarah L. Harris, Elsevier.	2012
2.	Fundamental of Logic Design - Charles H. Roth, and Larry L. Kinney, Brooks/Cole Inc.	2014
3.	Research and review paper in specific area.	

Equivalent MOOCs courses:

Sr. No.	**Course Links**	**Offered by**
1	System Design Through Verilog By Prof. Shaik Rafi Ahamed | IIT Guwahati https://onlinecourses.nptel.ac.in/noc24_ee94/preview	Swayam NPTEL
2	Digital System Design By Prof. Neeraj Goel | IIT Ropar https://onlinecourses.nptel.ac.in/noc24_ee17/preview	Swayam NPTEL

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	H	H	H	M	M
CO2	H	H	H	H	H	H
CO3	H	H	H	M	H	M
CO4	H	H	H	H	H	H
CO5	H	H	H	H	H	H

Course Name	**:**	**SEMICONDUCTOR DEVICE MODELING**
Course Code	**÷**	**EV1105**
Credits	**÷**	**3**
L T P	**÷**	**2 0 2**

Course Objectives:

Students should be able

- To understand the detailed Energy Band Diagrams for Semiconductor Devices.
- To explain the equations, approximations and techniques available for deriving a model and apply suitable approximations and techniques to derive the model referred to above starting from drift-diffusion transport equations.
- To analyze the device behavior through Semiclassical transport approach.
- To understand the fundamentals of compact modeling.

Total No. of Lectures: 28

Lecture wise breakup		**No. of hrs.**
Unit 1	**ENERGY BAND DIAGRAMS** Wave nature of electrons, carrier momentum and energy, excess EHP concentration, crystal momentum, effective mass, group velocity and crystal momentum of electron, ε-k and ε-x diagrams of semiconductor	4
Unit 2	**DRIFT DIFFUSION MODELLING** Drift-Diffusion Model Derivation and dielectric relaxation time, Taylor series expansion and Finite Difference method, Scaling and Linearization of Poisson's, Generation and Recombination models, Derivation of SRH model, Boundary conditions	5
Unit 3	**SEMI-CLASSICAL BULK TRANSPORT** Mechanisms of carrier motion as semi-classical, concepts of scattering, the phenomena of ohmic transport, velocity saturation, velocity overshoot and ballistic transport of carriers, drift diffusion carrier transport formulation from carriers as particles in random thermal motion, Maxwell's wave equations, Newton's second law and Boltzmann Transport Equation (BTE)	6
Unit 4	**HYDRODYNAMIC MODELING** As extension of DD model, Carrier Balance, Energy balance and momentum balance Equations, Direct solution scheme through Monte Carlo simulations	6
Unit 5	**COMPACT MODELING** Basic principles of physical device simulation (TCAD) and compact models, application of compact model, existing industry-standard compact models, implementation of compact models using hardware descriptive languages (Verilog-A), Verilog-A details and coding practices, mathematics for compact modeling	7

List of Experiments		**No. of turns**
1.	Introduction to TCAD software-meshing, models, parameters selection, TCL scripting	2
2.	Design PN-junction diode and simulate IV and CV characteristics incorporating Drift-Diffusion Models	3
3.	Design a MOSFET and simulate IV and CV characteristics for different channel lengths and incorporate different Models as transistor scales.	3
4.	Perform ballistic transistor simulations models using MATLAB. Also incorporate Monte carlo models and compare results.	3
5.	Write a Verilog A model for nMOS characteristics and interface with cadence using compact modeling models.	3

Course Outcome: By the end of the course, student will be able to:	
1	Plot and extract parameters from the Energy Band Diagrams.
2	Apply the classical, semi-classical and quantum modeling concepts for various semiconductor devices.
3	Perform and analyze the results through monte carlo simulations.
4	Built the fundamentals of compact models for various semiconductor devices.

Suggested Books:

Text books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	M. Lundstrom, "Fundamentals of Carrier Transport", Cambridge University Press, 2000.	2000
2	Snowden, "Introduction to Semiconductor Device Modeling", World Scientific, 1986.	Latest Edition
3	S.M. Sze, Kwok K. Ng "Physics of Semiconductor Devices".	Latest Edition
Reference books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Y. Tsividis and C. McAndrew, "MOSFET modeling for Circuit Simulation", Oxford University Press, 2011.	2011
2	BSIM Manuals available on BSIM homepage on the internet.	---
3	Semiconductor optoelectronic devices: Pallab Bhattacharya, Pearson.	2008

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	Semiconductor Device Modeling, IIT Madras https://archive.nptel.ac.in/courses/117/106/117106033/	**NPTEL**

CO-PO Mapping:

Cos	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	H	M
CO2	H	M	H	H	H	M
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	M

Course Name	**:**	**ANALOG AND MIXED SIGNAL VLSI DESIGN**
Course ID	**:**	**EV1106**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Course Objectives:

Students should be able

- To understand the fundamental principles and methodologies involved in analog and mixed-signal IC design using CMOS technologies.
- To learn about the operation of MOS based amplifiers, current mirror and analyze their performance characteristics
- To design MOS based operational amplifier and evaluate its frequency response and related parameters
- To understand the basic concept of sample-hold circuit, A/D, D/A converters.

Total No. of Lectures- 28

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** Introduction to Analog IC Design, Analog ICs Design flow, MOS Characteristics and Parameters, MOSFET Models, MOS Diode, MOS Capacitors, MOS Switches, Noise in MOSFETs.	5
Unit 2	**CMOS AMPLIFIERS** Single stage amplifiers: CS, CG and CD stages, Small Signal Models, Input Output Impedances, and Frequency Response. Differential Amplifier, Cascode Amplifiers, Current Amplifiers, Current Sinks and Sources, current Mirrors, Wilson Current Mirror, and High Swing Current Mirror, Band gap Reference.	7
Unit 3	**CMOS OPERATIONAL AMPLIFIERS** Introduction and Design of CMOS Op-Amps, Compensation of CMOS Op Amps, Design of single and Two-Stage Op-Amps, Common-mode Rejection Ratio (CMRR), Power- Supply Rejection Ratio (PSRR), Cascode Op-Amps, and Characterization Techniques of OP-Amps.	8
Unit 4	**MIXED-SIGNAL CIRCUITS** Sample-and-Hold, Implementation of S/H, PLL, LDO, Buck boost Converter, Charge Pump circuits & Application, Analog Filters: Integrator building blocks, MOSFET-C Integrator Discrete time Integrators, Filtering topologies, Bilinear and Biquadratic Transfer function, Digital Filters: Introduction to Digital-to-analog Converters, Analog-to-Digital Converters.	8

List of Experiments		**No. of turns**
1	Obtain the characteristics of MOS current mirror using Cadence tool.	2
2	(a) Obtain the characteristics of CMOS based differential amplifier using Cadence tool. Perform AC analysis and calculate its gain margin and phase margin (b) Draw the layout of differential amplifier.	3
3	Obtain the characteristics of single stage and two stage MOS operational amplifier using Cadence tool. Perform AC analysis and calculate common mode gain, differential mode gain, CMRR, slew rate.	3

4	Draw the layout of single stage, two stage operational amplifier using Cadence virtuoso and perform DRC, LVS.	3
5	Design a single-stage CMOS operational amplifier to meet the following specifications: Voltage Gain (A_v): ≥ 60 dB, Slew Rate (SR): ≥ 10 V/µs, Load Capacitance (C_L): 5 pF, Supply Voltage (V_{DD}): 1.8 V, Technology Node: 180 nm CMOS.	3

Course Outcomes: By the end of this course, the students will be able to	
1	Explain the fundamentals of analog and mixed VLSI circuits, and their small signal models.
2	Analyze the operation of MOS differential amplifier and current mirrors.
3	Design and evaluate MOS-based operational amplifier using CAD tools.
4	Analyze the concept of mixed-signal integrated circuits with their performance parameters.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill	2008
2	Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley	2004
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Johns, D.A. and Martin, K., Analog Integrated Circuit Design, John Wiley	2008

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	Analog IC Design https://archive.nptel.ac.in/courses/117/106/117106030/	**NPTEL**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	M	H
CO2	H	M	H	H	H	H
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	H

SEMESTER-II
DEPARTMENT ELECTIVE COURSES (DEC-II))

Course Name	**:**	**REAL TIME EMBEDDED SYSTEMS**
Course ID	**:**	**EV1251**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Course Objectives:

Students should be able

- To understand real time systems and related issues
- To explain the characteristics of latency in real time systems.
- To understand various processor architectures and their differences in terms of performance and application suitability
- To explore the principles and components of System-on-Chip (SoC) design

Total No. of Lectures – 28

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** Issues in real time computing, structure of a real time system. task classes. Characterizing real time Systems and tasks: Introduction, performance measures for real time systems: Traditional performance measures, performability, cost functions and hard deadlines.	8
Unit 2	**RTOS AND APPLICATION DESIGN** Real time operating systems, embedded. RTOS, real time process scheduling, structure of real time operating system, memory management in embedded operating system, overhead inter-process communication mechanisms, file systems in embedded devices, different types of locks, Semaphores. Real Time Communication: Introduction, architectural issues, protocols: deadlines based protocols, hierarchical round robin protocol, token based protocol.	7
Unit 3	**EMBEDDED PROCESSING** Introduction to embedded computing, difference between embedded and general purpose computing, characterizing embedded computing, design philosophies, RISC, CISC, VLIW versus superscalar, VLIW versus DSP Processors, register file design, pipeline design, the control unit, control registers, microprocessor versus microcontroller architecture. Embedded Processors: ARM architecture, assembly programming, input output interfacing, GPIO, LCD interfacing, peripherals, DDR memory, SDRAM, interrupts, timers, ARM memory interface, AMBA.	6
Unit 4	**SYSTEM-ON-CHIP (SOC)** System-on-Chip (SoC), IP blocks and design reuse, processor cores and SoC, Non-programmable accelerators, reconfigurable logic. Mixed signal architectures and multiprocessor architectures. Multiprocessing on a chip, symmetric multiprocessing, heterogeneous multiprocessing, validation and verification, hardware software partitioning, co-design.	7

List of Experiments:	**No. of turns**

1.	To program and simulate ARM processor-based experiments using flowcode.	5
2.	Develop a project using real time processor	5
3.	Case study with the latest tools available in the respective lab.	4

Course Outcomes: By the end of this course, the students will be able	
1.	To understand the basics and importance of real-time systems
2.	To understand multi-task scheduling algorithms for periodic, aperiodic, and sporadic tasks as well as understand the impact of the latter two on scheduling.
3.	To realize practical aspects like input/output interfacing, peripheral integration
4.	To understand the reconfigurable logic, mixed-signal architectures, and multiprocessor architectures, including the concepts of symmetric and heterogeneous multiprocessing

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Embedded System Design by Santanu Chattopadhya, Second Edition.	2013
2	Phillip A. Laplante, Real-Time Systems Design and Analysis, Wiley Publishers 4th edition	2011
3	Embedded system architecture by Raj Kamal, 2nd edition, Tata McGraw Hill	
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Real-Time Systems, Jane W. S. Liu, Pearson Education Asia	2003
2	Qing Li, Caroline Yao, Real-Time Concepts for Embedded Systems, CRC Press	2003
3	Research and review papers in specific area.	

Equivalent MOOCs courses:

Sr. No.	**Course Links**	**Offered by**
1	Embedded Systems (IIT Kharagpur) By Prof. Rajib Mall, Prof. Amit Patra, Prof. A. Routray https://nptel.ac.in/courses/108105057	**NPTEL**
2	Embedded system design with ARM, IIT Kharagpur Prof. Indranil Sengupta https://archive.nptel.ac.in/courses/106/105/106105193/	**NPTEL**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	H	H	M	M	L
CO2	H	H	H	H	H	M
CO3	H	H	H	H	H	M
CO4	H	H	H	H	H	H

Course Name	**:**	**OPTOELECTRONIC MATERIALS AND DEVICES**
Course ID	**:**	**EV1252**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To understand basic optical systems and explore key properties of elemental and compound semiconductors used in optoelectronics.
- To understand light-matter interactions and optical properties of materials.
- To study the principles and structures of optical sources, photodetectors and solar cells
- To understand the principles, materials, and applications of photonic integrated circuits and nanophotonic devices.

Total No. of Lectures – 42

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION** Generic Optical Systems and Fundamental Building Blocks; Optoelectronic Materials: Basics of Semiconductor, Elemental and Compound Semiconductors.	3
Unit 2	**OPTICAL PROPERTIES** Electronic and Optical Properties in Semiconductors, Dielectrics and polymers; Ray optics, Electromagnetic optics and guided wave optics; Physics of light-matter interactions; 2D material photonic integration.	6
Unit 3	**OPTICAL SOURCE** Heterostructures, Component of Electron Waves, Optical Waveguides, Guided Modes, FabryPerot Lasers, Coupled Mode Theory, DBR and DFB Lasers, Modulation Bandwidth, LED structures and types, Materials for LED.	8
Unit 4	**PHOTODETECTORS AND SOLAR CELLS** General Characteristics of Photodetectors, Impulse Response, Photoconductors, PIN, APD, Array Detectors, CCD, Solar Cell: Device Physics of Solar Cells, Single, Tandem multi-junction solar cells, thin film solar cells: Amorphous silicon, Quantum Dot solar cells	7
Unit 5	**PHOTONIC INTEGRATED CIRCUITS** An introduction, Material technology for integrated optics, Optical interconnects, integrated photonic Passive devices, Integrated photonic Active devices, Photonic integrated circuit technology: Silicon, III-V and beyond, Application of Photonic circuit in Communication and Sensing.	10
Unit 6	**NANOPHOTONICS** Optical near fields and effective interactions as a base for nanophotonics – Principles of operations of nanophotonic devices using optical near fields, Principles of nanofabrication using optical near fields. Excitation energy transfer – Device operation: nanophotonic AND gate & nanophotonic OR gate.	8

Course Outcomes: By the end of this course, the students will be able to	
1	Understand the fundamentals of optical systems and optoelectronic materials, including elemental and compound semiconductors.
2	Analyze electronic and optical properties of materials and light-matter interactions in various optical regimes.
3	Explain the working principles of optical sources such as lasers and LEDs, and their design components.
4	Evaluate the operation of photodetectors and solar cells, including advanced structures and materials.
5	Apply concepts of photonic integration and nanophotonics in the design of optical circuits and nanoscale devices.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	C.P. Wong, Polymers for Electronic and Photonic Applications, Academic Press, 1993.	Latest Edition
2	S.O. Kasap, P. Capper, Handbook of Electronic and Photonic Materials, Springer, 2006.	Latest Edition
3	A. Yariv and P. Yeh, "Photonics, 6th edition, Oxford, 2007.	2007
4	S.O. Kasap, Optoelectronics and Photonics: Principles and Practices, Pearson Education, 2009.	2009
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Nano Photonics; P N Prasad, Wiley Interscience (2003)	Latest edition
2	Photonic Devices. Cambridge, J. Liu, Cambridge University Press (2005)	2005
3	Principles of Nanophotonic, Motoichi Ohtsu et al., CRC Press-Taylor & Francis Group, NY, USA (2008)	2008

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	https://archive.nptel.ac.in/courses/118/106/118106021/	**NPTEL**
2	https://onlinecourses.nptel.ac.in/noc21_ee35/preview	**NPTEL**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	H	M
CO2	H	M	H	H	H	H
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	M
CO5	H	M	H	H	H	M

Course Name	**:**	**SEMICONDUCTOR PACKAGING**
Course ID	**:**	**EV1253**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To analyze the basics of electronic device packaging and testing.
- To gain the knowledge for designing ICs for various applications.
- To examine the role of interconnections and assembly materials to meet electrical and mechanical requirements.
- To develop an understanding of inter-disciplinarity of packaging involving electrical, mechanical, thermal, materials, and processes.

Total No. of Lectures – 42

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION TO SEMICONDUCTOR PACKAGING** Definition of packaging and its significance in various industries; Introduction to packaging and its importance in Modern Electronics. Traditional packaging technologies: Leaded and leadless packages.	8
Unit 2	**PACKAGE MANUFACTURING PROCESSES:** Packaging Assembly Technology, Wafer Thinning, Dicing, Die Attach, Wire bonding, Flip Chip process, Flux Cleaning, Underfill, Encapsulation, Laser Marking, Solder Ball Attach, Reflow, Singulation, IC Packaging Toolsets & equipment operation, clean room operations.	5
Unit 3	**SEMICONDUCTOR COMPONENT AND PACKAGE TEST** Overview of Testing methodologies, components tested & their characteristics, Challenges in testing, Types of Testers (Automated test Equipment & Benchtop Testers), Components & Subsystems of Testers, Principles of Functional Testing, Parametric/ Boundary Scan /In-Circuit Test/ Flying Probe Test, Test Data Analysis, Design for Testability & Tester Calibration & Maintenance, Future Trends.	10
Unit 4	**ELECTRICAL AND PHYSICAL FAILURE ANALYSIS** Package failure modes, Failure detection mechanisms, Failure analysis tools, Test programs debugging, Data Analytics, ESD & EMI Management.	8
Unit 5	**SEMICONDUCTOR PACKAGE MATERIALS AND QUALIFICATION** Reliability testing & qualification- MST/MSL, TC/TS, HAST & uHAST, Mold Compounds (Moldability), Underfill Materials, Die Attach Adhesives & Films, Substrate Technology, Bonding Wire, Solder & Dielectric materials.	5
Unit 6	**INDUSTRIAL QUALITY AND STATISTICAL PROCESS CONTROL** Quality Control Plan (QCP) & Quality Management System (QMS), Incoming Material Inspection, In-Line Quality, Measurement System Analysis, Statistical analysis methods, Statistical Process Control (SPC), Fault Detection Control (FDC), Run-to-Run Control (R2R), Auto Defect Classification (ADC), Data Analytics, Machine Communication Protocol and System Integration.	6

Course Outcomes: By the end of this course, the students will be able to	
1	Comprehend the manufacturing process of various semiconductor packages.
2	Describe various package materials, their testing and failure analysis.
3	Explain the package qualification methods and industrial quality management for the same.
4	Explain EMI and ESD effects, test program analysis and statistical process control of package

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Semiconductor Packaging: Materials interaction and reliability, Andrea Chen and R. Yu Lo, CRC.	2012
2	Semiconductor Manufacturing, H. Geng, TMH.	Latest edition
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Gary S. May, Costas J. Spanos, Fundamentals of Semiconductor Manufacturing and Process Control (Wiley - IEEE)	2006
2	Semiconductor advanced packaging, John H. Lau, Springer.	2021

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	Electronic Manufacturing and Packaging https://nptel.ac.in/courses/112105267	**NPTEL**
2	Intro to Electronic Packaging https://ep.jhu.edu/courses/525607-intro-to-electronic-packaging/	**Johns Hopkins University, US**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	H	H	H	H	H
CO2	H	H	M	H	H	H
CO3	H	H	M	H	M	H
CO4	H	H	M	H	M	H

Course Name	**:**	**RADIO FREQUENCY INTEGRATED CIRCUIT (RFIC)**
Course ID	**:**	**EV1254**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To understand fundamental principles of RF circuits, systems, and impairments such as noise and distortion.
- To develop an understanding of CMOS RFIC components, layouts, and performance analysis using *S*-parameters and noise figures.
- To design and evaluate low-noise and power amplifiers with advanced techniques for noise and linearity improvement.
- To explain RF mixers, oscillators, and frequency synthesizers and their applications.

Total No. of Lectures – 42

Lecture wise breakup		**No. of Lectures**
Unit 1	**FUNDAMENTALS OF RF CIRCUITS AND SYSTEMS** Basic concepts of Linearity, Nonlinearity, Time Variance, Inter-symbol Interference, Random Processes, and Noise. Definitions of Sensitivity and Dynamic Range, Conversion Gains, and Distortion. Analog and Digital Modulation for RF Circuits, Review of modulation schemes, Receiver architectures, Transmitter architectures.	11
Unit 2	**PASSIVE AND ACTIVE COMPONENTS FOR CMOS RFIC** RF Transistor Layout, CMOS Technology for RF, CMOS Circuit Design: Capacitors, Varactors, Resistors, Inductors, Transformers, Transmission lines Resonance, Matching, *S*-parameters, etc. Noise in Electrical Circuits and NF Calculations, Two Port Noise Theory.	11
Unit 3	**AMPLIFIERS** Low Noise Amplifiers: Resistive Terminated CS and CG LNA, Inductive Degenerated LNA, Shunt feedback LNA, Noise Canceling LNAs, Linearity Improvement Techniques. Power Amplifiers: Power Combining, Linearity Improvement Techniques.	10
Unit 4	**MIXERS, OSCILLATORS, FREQUENCY SYNTHESIZERS** Mixers: Introduction, Specifications, NL System as a Mixer, Active Mixers, Passive Mixers. Oscillators: Introduction, Types of Oscillators, Phase Noise. Frequency Synthesizers: Principles, Design, Integer N and Fractional Synthesizers, Dividers.	10

Course Outcomes: By the end of this course, the students will be able to	
1	Demonstrate understanding of RF circuit fundamentals, system impairments, and modern RF architectures.
2	Analyze CMOS RFIC passive and active components, and evaluate performance metrics such as noise figure.
3	Design and assess LNAs and PAs with advanced techniques to improve noise and linearity.
4	Develop and evaluate RF mixers, oscillators, and frequency synthesizers with focus on phase noise and tuning.

Suggested Books:

Text Books		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication / Reprint**
1	Behzad Razavi, "RF Microelectronics", 2nd Ed., Pearson.	2012
2	Thomas H. Lee, "The design of CMOS radio-frequency integrated circuits", 2nd Ed., Cambridge University Press.	2004
Reference Books		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication / Reprint**
1	Bosco Leung, "VLSI for Wireless Communication", Personal Education Electronics and VLSI series, Ed: Chharles G. Sodini, Pearson Education.	2002
2	John W. M. Rogers and Calvin Plett, "Radio Frequency Integrated Circuit Design", Artech House.	2010
3	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Ed., McGraw Hill Education.	2017
4	Relevant Research Papers.	

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	RF Integrated Circuits by Dr. Shouribrata Chatterjee, Department of Electrical Engineering, IIT Delhi. https://archive.nptel.ac.in/courses/117/102/117102012/#	**NPTEL**

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	M	M
CO2	H	M	H	H	H	H
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	H

Course Name	:	**CAD for VLSI**
Course Code	:	**EV1255**
Credits	:	**3**
L T P	:	**2 0 2**

Course Objectives:

Students should be able

- To understand the fundamentals of Computer-Aided Design tools for the modeling, design, and analysis of VLSI systems.
- To learn programming using system Verilog.
- To analyze the Front- End and Back-End Design of VLSI.
- To get acquainted with the concepts of fault detection and testing of combinational and sequential circuits.

Total no. of lectures-28

Lecture wise breakup		**No. of Lectures**
Unit 1	**FRONT-END DESIGN** VLSI design flow, challenges, Different Stages in VLSI Design flow, Front end design flow, Hardware Description languages: An overview of system Verilog, Representation of sequential circuits by FSMs; optimization of FSMs; binary coding of FSMs.	6
Unit 2	**LOGIC SIMULATION AND LOGIC SYNTHESIS** Logic simulation, compiled and event simulators, relative advantages and disadvantages, Multilevel logic synthesis: Factoring and Functional Decomposition, Logic Optimization.	6
Unit 3	**BACK-END DESIGN** Review of MOS/CMOS fabrication technology, Layout Algorithms, Floorplaning, Floorplanning Algorithms, Circuit partitioning, Circuit partitioning Algorithms, Placement, and Routing algorithms; Design rule verification; Circuit Compaction; Circuit extraction and post layout simulation, power and delay estimation, clock and power routing.	7
Unit 4	**FAULT DETECTION AND TESTING OF COMBINATIONAL AND SEQUENTIAL CIRCUITS** Introduction to testing, Fault tables; Boolean difference; structure-oriented computation of Boolean difference; fault simulation; fault trees; D-Algorithm; testing of sequential circuits; Design for testability. Design for testability. Mixed Integer Linear Programming (MILP) Modeling: properties of modeling method, mathematical modeling techniques (constraint linearization, OR-relation transformation, propositional logic modeling, absolute value modeling), modeling common EDA problems including grid routing, gridless routing, escape routing on printed circuit board (PCB), area routing on PCB, non-overlapping placement, area minimization, network flow.	9

List of Experiments		**No. of Turns**
1	Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND, OR gates. Write test bench with appropriate input patterns to verify the modeled behavior.	2
2	Design 2x1 mux using Verilog and write test bench.	2
3	Design 2x4 decoder using Verilog and write test bench.	2
4	Design 4-bit up-down counter using Verilog and verify its functioning using ISE simulator.	2
5	Write Verilog code and verify functionality for frequency divider circuit.	2
6	Write Verilog code using FSM to simulate elevator operation.	4

Course Outcomes: By the end of the course, students will be able to:	
1	Explain the concepts of system Verilog.
2	Perform simulation and synthesis of various combinational and sequential circuits using system Verilog.
3	Explain various phases of Front-End and Back-End Design of VLSI circuits.
4	Understand and analyze fault detection and testing of combinational and sequential circuits.

Suggested Books:

Text books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Algorithms for VLSI Design Automation, S.H. Gerez, Addison-Weseley Longman Singapore Private Limited.	2008
2	Algorithms and Techniques for VLSI Layout Synthesis, Hill, D., D. Shugard, J. Fishburn and K. Keutzer, Kluwer Academic Publishers, Boston.	1989
3	System verilog for verification, Chris Spear, Springer	2006
Reference books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Computer Aided Design and VLSI Device development, Kit Man Cham, Soo- Young Oh, Daeji Chin, John L. Moll, Springer.	2012
2	Algorithms for VLSI Physical Design Automation by Naveed A. Sherwani, Kluwer Academic Publishers.	2012
3	M.L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing, Kluwer Academic Publishers	2000

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	CAD for VLSI design-1, IIT Madras https://archive.nptel.ac.in/courses/106/106/106106088/	**NPTEL**

CO-PO Mapping:

COs	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	M	H	H	H	H
CO2	H	M	H	H	H	H
CO3	H	M	H	H	H	H
CO4	H	M	H	H	H	H

Course Name	**:**	**TESTING & FAULT TOLERANCE**
Course ID	**:**	**EV1256**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To identify the faulty chips after manufacturing.
- To generate test patterns for combinational circuits and to design DFT.
- To explore test pattern generation algorithms for sequential circuits.
- To understand Built-In Self-Test and fault tolerance in VLSI chips.

Total No. of Lectures – 42

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION TO TESTING** Introduction to Digital VLSI Testing, Functional and Structural Testing, Structural Testing with Fault Models, Fault Equivalence, Fault Dominance, Fault Collapsing.	5
Unit 2	**FAULT SIMULATION** Fault Simulation, Circuit Simulation, Serial, Deductive, Parallel, and Concurrent Fault Simulation, Critical Path Tracing, SCOAP Rules to Compute Combinational Controllability and observability.	8
Unit 3	**ATPG FOR COMBINATIONAL CIRCUITS** ATPG algebra, D- Algorithm, Boolean difference, Path sensitization, Podem, Random, Deterministic and Weighted Random Test Pattern Generation.	8
Unit 4	**PLA AND MEMORY TESTING** PLA Testing, Cross Point Fault Model and Test Generation, Memory Testing - Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests.	8
Unit 5	**ATPG FOR SEQUENTIAL CIRCUITS** Time Frame Expansion, Scan Chain Based Testing, BILBO, Boundary Scan for Board Level Testing, Built in Self-Test and Totally Self checking Circuits.	8
Unit 6	**FAULT TOLERANCE** Introduction to the concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes, Reconfiguration Techniques, Yield Modelling Reliability and Effective Area Utilization.	5

Course Outcomes: By the end of this course, the students will be able to	
1	Identify the significance of testable design and generate the test pattern for Structure testing.
2	Analyze the fault model, fault coverage and fault simulation.
3	Generate the test patterns for PLA and memory chips.
4	Implement combinational and sequential circuit test generation algorithms.
5	Design the appropriate circuit to embed fault-tolerant techniques.

Suggested Books:

Textbooks:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Bushnell, M. and Agrawal, V.D., Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits, Kluwer Academic.	2000
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Abramovici M., Breuer M. A. and Friedman A.D., Digital Systems Testing and Testable Design, Jaico Publishing House.	2001
2	Pradhan, D.K., Fault Tolerant Computer System Design, Prentice Hall.	1996
3	Latest Research and Review papers.	

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	Design Verification and Test of Digital VLSI Circuits, IIT Guwahati Prof. Jatindra Kumar Deka, Dr. Santosh Biswas https://nptel.ac.in/courses/106103116	**NPTEL**

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	L	M	L	L	L	L
CO2	M	M	M	M	M	M
CO3	M	H	M	M	H	H
CO4	H	H	H	H	H	H
CO5	H	H	H	H	H	H

OPEN ELECTIVES

Course Name	**:**	**NEURAL NETWORKS**
Course Code	**:**	**EV 3001**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To introduce some of the fundamental techniques and principles of neural computation.
- To understand the basic neural network models, single and multilayer perceptron.
- To investigate some associative Networks.
- To introduce some of neural networks based on competition.

Total No. of Lectures: 42

Lecture wise breakup		**No. of Lecture**
Unit 1	**INTRODUCTION TO NEURAL NETWORKS** Introduction to artificial neural networks, biological neural networks, comparison between biological and artificial Neural Networks, terminology and various architectures of Neural Networks, History of Neural Networks.	3
Unit 2	**FUNDAMENTAL CONCEPTS** MC Culloch-Pitt Neuron model, various Activation functions, Hebbnet, Biases and threshold, Linear separability.	4
Unit 3	**PATTERN CLASSIFICATION** Perceptron, Adaline and Madaline. Architecture, training algorithms and application algorithms of these networks, practical implementation using matlab.	7
Unit 4	**PATTERN ASSOCIATION** Architecture, Training and application Algorithms for Pattern Association networks, Heteroassociative Memory Neural Network, auto associative Net, Iterative Auto associative Net, Bidirectional Associative Memory, Discrete Hopfield Network, practical implementation of these networks using matlab.	7
Unit 5	**COMPETITIVE NETS** Maxnet, Mexican Hat, Hamming Net, Kohonen Self Organizing Maps, Learning Vector Quantization, Full and Forward Counterpropagation. Application based on these networks. Use of Counterpropagation net for a mathematical function, practical implementation using matlab.	7
Unit 6	**ADAPTIVE AND BACKPROPAGATION NETWORKS** Adaptive Resonance Theory: Introduction, architecture, algorithm and application of ART1. Backpropagation neural net, architecture, algorithm, variations, applications, derivation of learning rules. Applications based on backpropagation neural net.	7
Unit 7	**FIXED WEIGHT NETWORKS** Fixed-Weight Nets for Constrained Optimization, Neural Net approach to Constrained Optimization, Boltzmann Machine: architecture, algorithm, Travelling Salesman Problem. Examples based on Boltzmann Machine.	7

Course Outcomes: By the end of the course, the students will be able	
1	To implement neural networks for pattern classification.
2	To adequate knowledge about activation functions used for neural networks.
3	To design a fault tolerant neural network for character recognition.
4	To apply the concepts of neural networks to generate functions.

5	To design multi-layered neural networks to solve complex problems.
6	To solve complex problems using fixed weight neural networks like Travelling Salesman Problem.

Suggested Books:

Text Books:		
S. No.	**Name of the book/authors/ publisher**	**Year of publication/re print**
1.	Fundamentals of Neural Networks, Laurence Fausett, Pearson Education.	2006
2.	Neural networks and Fuzzy Logic, K Vinod Kumar, R. Saravana Kumar, Katson Books.	2012
3.	Neural Networks and machine learning, Haykin, Pearson Education.	2008
4.	Neural Networks, Satish Kumar, TMH.	2001
5.	Introduction to Neural Networks using MATLAB 6.0, S. N. Sivanandam, S. Sumathi and S.N. Deepa, Mc Graw Hill.	2006

Equivalent MOOCs Courses:

Sr. No.	**Course Links**	**Offered by**
1	RF Neural Networks and Applications, IIT Kharagpur Prof. Somnath Sengupta https://nptel.ac.in/courses/117105084	**NPTEL**

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	M	L	M	L	L	L
CO2	M	L	M	M	M	M
CO3	H	L	H	M	H	M
CO4	H	L	M	H	H	M
CO5	H	L	H	H	H	M
CO6	M	L	H	M	M	M

Course Name	**:**	**FLEXIBLE ELECTRONICS**
Course Code	**:**	**EV 3002**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To gain fundamental knowledge of thin-film materials and device physics for flexible and printed electronics.
- To describe key printing and deposition techniques for fabricating flexible devices.
- To perform circuit-level implementation and system integration on flexible substrates.
- To explore real-world applications, challenges, and future directions in flexible electronics and packaging.

Total No. of Lectures- 42

Lecture Wise Breakup		**No. of Lecture**
Unit 1	**INTRODUCTION TO FLEXIBLE AND PRINTED ELECTRONICS** Evolution of flexible electronics, review of cutting-edge research on flexible, plastic, stretchable, conformable or printed electronics. materials, components, and systems, applications for IoT.	**8**
Unit 2	**MATERIALS, PROCESSING, AND MANUFACTURING** Various semiconductors, dielectric, and conducting materials, Organic semiconductors; From chemical bonds to bands, Charge injection and transport, Examples of printable functional materials, Thin-film Deposition and Processing Methods for Flexible Devices, Solution-based Patterning Processes; Ink-jet printing, gravure and other processes, surface energy effects, multilayer patterning.	**12**
Unit 3	**FLEXIBLE THIN-FILM TRANSISTORS AND CIRCUITS** Thin-Film Transistor; Device structure and performance, Electrical characteristics, parameter extraction, characterization methods for rigid and flexible devices, electrical stability, printed transistors; Organic/polymer, metal-oxide, electrolyte gated, submicrometric OTFTs and gravure printed OTFTs, From transistors to circuits, circuits on flexible and non- silicon substrates, Contacts and Interfaces to Organic and Inorganic Electronic Devices, Schottky contacts, defects, carrier recombination, effect of applied mechanical strain.	**12**
Unit 4	**OTHER FLEXIBLE DEVICES AND SYSTEM INTEGRATION** Organic Light Emitting Diodes, flexible OLED displays and lighting, smart wallpaper, Organic Solar Cells, sensors, flexible batteries, supercapacitors, logic, memory, RFID tags, Latest applications, Encapsulation, roll to roll processes, Integration Issues, Designs for Future and case studies.	**10**

Course Outcome: By the end of this course, the students will be able to	
1	Explain the principles, materials, and physics behind thin-film and organic electronic devices used in flexible electronics.
2	Demonstrate knowledge of solution-based patterning, printing, and coating techniques and their applications in device fabrication.
3	Analyze and design thin-film transistors and circuits on flexible substrates, including the challenges in electrical characterization and mechanical strain.
4	Evaluate system-level integration, encapsulation, and performance issues in emerging flexible electronic applications like displays, sensors, and energy devices.

Suggested Books:

Text books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	"Large Area and Flexible Electronics", M. Caironi and Y.Y. Noh, WILEY-VCH.	2015
2	"Flexible Electronics: Materials and Applications", W. S. Wong, A. Salleo, Springer.	2009
Reference Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	Organic and Printed Electronics: Fundamentals and Applications, G. Nisato, D. Lupo, S.Ganz, CRC Press.	2016
2	Organic Flexible Electronics: Fundamentals, Devices, and Applications, P. Coseddu and M. Caironi, Elsevier.	2020
3	Christoph Brabec, Ullrich Scherf, Vladimir Dyakonov (Editors), Organic Photovoltaics: Materials, Device Physics, and Manufacturing Technologies, Wiley VCH.	2014

Equivalent MOOC courses:

Sr. No.	**Course Links**	**Offered by**
1	Not Available	

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	H	H	M	H	H	M
CO2	H	H	M	H	H	M
CO3	H	H	M	H	M	M
CO4	H	H	M	H	M	M

Course Name	**:**	**NEUROMORPHIC ENGINEERING**
Course Code	**:**	**EV3003**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To learn Ultra-low power computing electronics concepts mimicking computing by biological neurons.
- To develop a grasp of different Design and simulation techniques of CMOS and nano electronic circuits modelling biological brain.
- To understand Commercial neuromorphic systems and processors for machine learning applications.
- To acquire a basic knowledge of Future Trends in neuromorphic engineering Technology, as well as the commercialization paths for new materials, methods, and tools for neuromorphic electronic systems design.

Total number of Lectures-42

Lecture wise breakup		**No. of Lectures**
Unit 1	**INTRODUCTION TO CLASSIC NEUROMORPHIC CIRCUITS** Signaling and operation of biological neurons, neuron models, signal encoding and statistics; Synapses and plasticity rules, biological neural circuits.	**8**
Unit 2	**MOSFETS FOR NEUROMORPHIC ELECTRONICS** FETs - device physics and sub-threshold circuits.	**6**
Unit 3	**ANALOG AND DIGITAL ELECTRONIC NEURON DESIGN**	**6**
Unit 4	**PROGRAMMABLE NEUROMORPHIC CIRCUITS AND SYNAPSES** S piking Neural Network, Non-volatile memristive semiconductor devices; Electronic synapse design; Interconnection Networks; Interconnection schemes for large non-spiking and spiking neural networks.	**12**
Unit 5	**ANALOG AND DIGITAL NEUROMORPHIC CIRCUIT AND SYSTEM DESIGN** Analysis of design, architecture and performance characteristics of demonstrated chips employing Analog neuromorphic and Digital neuromorphic VLSI, Electronic synapses and other neuromorphic systems.	**10**

Course Outcomes: By the end of this course, the students will be able to	
1	Build power-saving hardware devices to analyse real-world noisy data utilizing brain-like mechanisms.
2	Identify and learn basic concepts and current trends in neuromorphic device, circuit, and system design.
3	Design, Develop and Document Analog and Digital neuromorphic systems.
4	Apply neuromorphic systems to develop new VLSI circuits and make report on the same.
5	The students will learn how electronics circuits mimic biological neurons, and will explore their novel variations in these circuits.

Suggested Books:

Text Books

Sr.No.	**Name of Book/ Authors/ Publisher**	**Year of Publication / Reprint**
1	Shih-Chii Liu, Jörg Kramer, Giacomo Indiveri, Tobias Delbrück, Rodney Douglas, Analog VLSI: circuits and principles, MIT press, ISBN 0262122553	2002
2	CarverMead, Analog VLSI and neural systems, Addison-Wesley, ISBN0201059924	1989
3	Eric Kandel, James Schwartz, Thomas Jessell, Steven Siegelbaum, A.J. Hudspeth, Principles of neural science, McGraw Hill, ISBN 0071390111	2012

4	Dale Purves, Neuroscience, Sinauer, ISBN 0878936971	2008

Equivalent MOOC courses:

Sr. No.	Course Links	Offered by
1	Not Available	

CO-PO Mapping:

CO	PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	-	-	H	L	L	L
CO2	-	-	H	M	M	M
CO3	M	H	H	M	H	M
CO4	M	H	H	H	H	M
CO5	M	-	H	H	H	M

Course Name	**:**	**SENSORS AND ACTUATORS**
Course Code	**:**	**EV3004**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Course Objectives:

Students should be able

- To understand sensors, how to fabricate the sensors and its application in real world.
- To design modern day microsensors and micro actuators.
- To create sensor modules in EDA/TCAD tools simulate them for correct operations before fabricating it.

Total No. of Lectures: 42

Lecture wise breakup		**No. of Lectures**
Unit 1	Basics of Energy Transformation, Transducers, Sensors and Actuators	3
Unit 2	Thin film physics, Application in MOSFET and its variants	4
Unit 3	Thin Film Deposition Techniques: Chemical Vapor Deposition (APCVD, LPCVD, UHVCVD, PECVD, ALCVD, HPCVD, MOCVD), Physical Vapor Deposition (Thermal Deposition, E-beam Evaporation, Sputtering, Pulsed Laser Deposition), Basic understanding of Photolithography for pattering layer. Detailed overview of Etching methods.	6
Unit 4	Gas sensors: Optical gas sensor, Metal oxide semiconductor gas sensor, Field effect transistor gas sensor, Piezoelectric gas sensor, Polymer gas sensor, Nano-structured based gas sensors, Design and fabrication process of Microsensors: Force Sensors, Pressure Sensors, Strain gauges and practical applications	8
Unit 5	Actuators: Piezoelectric and Piezoresistive actuators, micropumps and micro actuators with practical applications, basics of microfluidics to assist Photomask design using Clewin Software, pattern transfer techniques, PDMS moulding and degassing, device bonding techniques.	8
Unit 6	Interfacing: Sensor Interfacing with Microprocessor to build electronic system, Static and Dynamic Characteristic Parameters for Sensors and Actuators, Calibration of Sensor based electronics systems	8
Unit 7	Static and Dynamic Characteristic Parameters for Sensors and Actuators, Calibration of Sensor based electronics systems	5

Course Outcomes: By the end of this course, the students will be able to	
1	Explain fundamental physical and technical base of sensors and actuators.
2	Describe basic laws and phenomena that define behaviour of sensors and actuators.
3	Analyse various premises, approaches, procedures and results related to sensors and actuators.
4	Create analytical design and development solutions for sensors and actuators and present a report of the same.
5	Understand the functions of sensors, actuators and associated control systems for real time applications.

Suggested Books:

Text Books		
Sr. No.	**Name of Book/Authors/Publisher**	**Year of Publication /Reprint**
1	Sensors and Signal Conditioning Wiley-Blackwell.	2008
2	Jacob Fraden, Handbook of modern sensors, Springer, Stefan Johann Rupitsch.	Latest edition
3	Piezoelectric Sensors and Actuators: Fundamentals and Applications, Springer, 2018 Senturia S. D.	2018
4.	Microsystem Design, Kluwer Academic Publisher, 2001 J.D. Plummer, M.D. Deal, P.G. Griffin.	2001
5	Silicon VLSI Technology, Pearson Education, 2001 S.M. Sze (Ed).	2001
6	VLSI Technology, 2nd Edition, McGraw Hill, 1988 Madou.	Latest edition
7	M Fundamentals of Microfabrication, CRC Press, 1997.	Latest edition

Equivalent MOOC courses:

Sr. No.	**Course Links**	**Offered by**
1	Sensors and Actuators By Prof. Hardik Jeetendra Pandya, IISc Bangalore https://onlinecourses.nptel.ac.in/noc21_ee32/preview	**NPTEL**

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	-	-	H	L	L	L
CO2	-	-	H	M	M	M
CO3	L	-	H	M	H	M
CO4	M	M	H	H	H	M
CO5	M	M	H	H		M