IEEE Chandigarh Subsection

PEC EXPLORE INNOVATE EXCEL

ISSE Indian Society of Systems for Science and Engineering

One Day National Seminar

on

Semiconductor Technology: Trends and Challenges

In technical collaboration with IEEE Chandigarh Subsection and ISSE Chandigarh Chapter

Supported by: Technical Education Quality Improvement Programme (TEQIP)-III

May 12, 2018

TECHNICAL SCHEDULE

	Registration	**09:00-09:30**
Welcome Address	**Arun Kumar Singh, Coordinator, Seminar**	**09:40-09:45**
	Neelu Jain, Head, ECE Dept.	**09:45-09:50**
	H S Jatana, President, ISSE Chandigarh Chapter	**09:55-10:00**
Lecture 1	**H S Jatana, SCL Mohali** *Semiconductor Technology – Opportunities & Challenges (India Perspective)*	**10:00-11:00**
	Tea Break	**11:00-11:15**
Lecture 2	**Satinder K Sharma, IIT Mandi** *F RAM and EUV- Resists: Changing the Integrated Circuits Fab. Landscape for Next Generation Technology node*	**11:15-12:15**
Lecture 3	**Avinash Singh, SCL Mohali** *SOI Technology*	**12:15-13:15**
	Lunch Break	**13:15-14:15**
Lecture 4	**Manish K Hooda, SCL Mohali** *Compound Semiconductor Technologies: Applications and Process Approach*	**14:15-15:15**
Lecture 5	**D S Rawal, SSPL Delhi** *Recent trends in Wide Bandgap Device Technology for Microwave Applications*	**15:15-16:15**
	Tea Break	**16:15-16:30**
Lecture 6	**Krishan Kumar, SCL Mohali** *Advance Packaging Technologies: for CMOS Devices*	**16:30-17:30**
	Valedictory and Certificate Distribution	**17:30-17:50**
	Vote of Thanks	**17:50-18:00**